it. A synthesization circuit 107 generates a write address by combining the color plane head address received from the selector 105, the vertical address received from the vertical address counter 91 and the horizontal address received from the horizontal address counter 103, and registers it in a write address register 109. The write address that is registered in the write address register 109 is transmitted to the memory control circuit 19. The memory control circuit 19 writes, at the write address in the memory 21, the write data that are received from the raster data processing circuits 83 to 85 in Fig. 5. This writing process is effected by using new data to OR the data that are already present at the address.

IN THE CLAIMS:

Please add the following new claims:

31. (New) A printer ~~control circuit according to claim 1,~~ wherein the low-resolution raster data for the second image element is generated by ~~performing~~ a halftone process in said upper apparatus.

32. (New) A printer according to claim 11, wherein the low-resolution raster data for the second image element is generated by performing a halftone process in said upper apparatus.

33. (New) A printing system according to claim 21, wherein the low-resolution raster data for the second image element is generated by performing a halftone process in said upper apparatus.